

Dual Enhancement Mode Field Effect Transistor (N and P Channel)

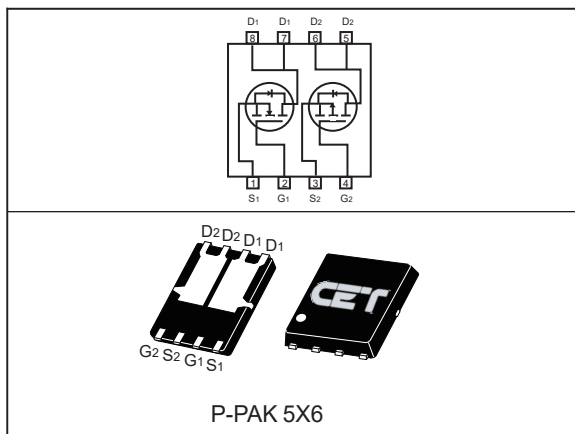
FEATURES

- High power and current handing capability.
- Reliable and rugged.
- Pb-free lead plating ; RoHS compliant.
- Halogen Free.
- Surface mount Package.

APPLICATIONS

- Synchronous Rectification.
- DC/DC converters.
- Motor Control.

	V_{DSS}	$R_{DS(ON)} \text{ typ@}V_{GS}$	I_D
N Channel	30V	$9.2\text{m}\Omega @ V_{GS} = 10\text{V}$	40A
P Channel	-30V	$12.5\text{m}\Omega @ V_{GS} = -10\text{V}$	-34A



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter		Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	± 20	± 20	V
Drain Current-Continuous	$I_D @ R_{\theta JC}$	$T_C = 25^\circ\text{C}$	40	-34	A
		$T_C = 70^\circ\text{C}$	32	-27	A
	$I_D @ R_{\theta JA}$	$T_A = 25^\circ\text{C}$	13	-11	A
		$T_A = 70^\circ\text{C}$	11	-9.1	A
Drain Current-Pulsed ^a	$I_{DM} @ R_{\theta JC}$	$T_C = 25^\circ\text{C}$	160	-136	A
	$I_{DM} @ R_{\theta JA}$	$T_A = 25^\circ\text{C}$	52	-44	A
Maximum Power Dissipation		P_D	27.8		W
Operating and Store Temperature Range		T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	4.5	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	40	$^\circ\text{C/W}$

N-Channel Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30V, V_{GS} = 0V$			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
On Characteristics ^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	1.3		3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 6A$		9.2	11.0	m Ω
		$V_{GS} = 4.5V, I_D = 3A$		11.0	14.3	m Ω
Gate input resistance	R_g	f=1MHz,open Drain		1.6		Ω
Dynamic Characteristics ^c						
Input Capacitance	C_{iss}	$V_{DS} = 15V, V_{GS} = 0V,$ f = 1.0 MHz		650		pF
Output Capacitance	C_{oss}			100		pF
Reverse Transfer Capacitance	C_{rss}			85		pF
Switching Characteristics ^c						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15V, I_D = 10A,$ $V_{GS} = 10V, R_{GEN} = 6\Omega$		17		ns
Turn-On Rise Time	t_r			7		ns
Turn-Off Delay Time	$t_{d(off)}$			23		ns
Turn-Off Fall Time	t_f			15		ns
Total Gate Charge	Q_g	$V_{DS} = 15V, I_D = 10A,$ $V_{GS} = 4.5V$		6.2		nC
Gate-Source Charge	Q_{gs}			1.6		nC
Gate-Drain Charge	Q_{gd}			3.6		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Current-Continuous	I_S				33	A
Drain-Source Diode Current-Pulsed ^b	I_{SM}				160	A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{GS} = 0V, I_S = 1A$			1.2	V
Notes : a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. c.Guaranteed by design, not subject to production testing.						

P-Channel Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30V, V_{GS} = 0V$			-1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
On Characteristics ^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = -250\mu A$	-1.3		-3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -7.5A$		12.5	15.0	m Ω
		$V_{GS} = -4.5V, I_D = -4A$		18.8	24.4	m Ω
Gate input resistance	R_g	f=1MHz,open Drain		6.3		Ω
Dynamic Characteristics ^c						
Input Capacitance	C_{iss}	$V_{DS} = -15V, V_{GS} = 0V,$ f = 1.0 MHz		1500		pF
Output Capacitance	C_{oss}			190		pF
Reverse Transfer Capacitance	C_{rss}			160		pF
Switching Characteristics ^c						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15V, I_D = -10A,$ $V_{GS} = -10V, R_{GEN} = 6\Omega$		17		ns
Turn-On Rise Time	t_r			10		ns
Turn-Off Delay Time	$t_{d(off)}$			45		ns
Turn-Off Fall Time	t_f			15		ns
Total Gate Charge	Q_g	$V_{DD} = -15V, I_D = -10A,$ $V_{GS} = -4.5V$		12		nC
Gate-Source Charge	Q_{gs}			3.3		nC
Gate-Drain Charge	Q_{gd}			6.5		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Current-Continuous	I_S				-33	A
Drain-Source Diode Current-Pulsed ^b	I_{SM}				-136	A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{GS} = 0V, I_S = -7.5A$			-1.3	V
Notes : a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. c.Guaranteed by design, not subject to production testing.						

N-CHANNEL

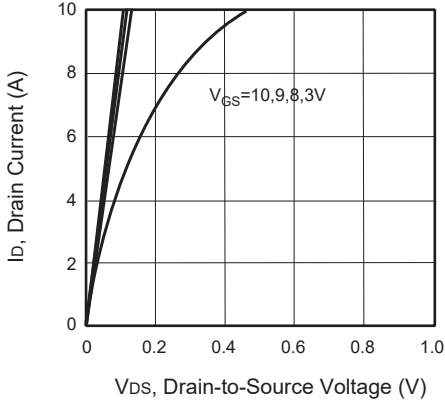


Figure 1. Output Characteristics

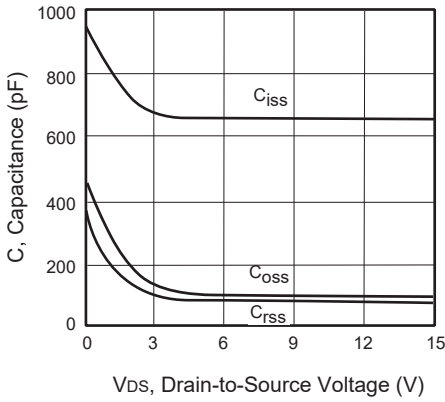


Figure 3. Capacitance

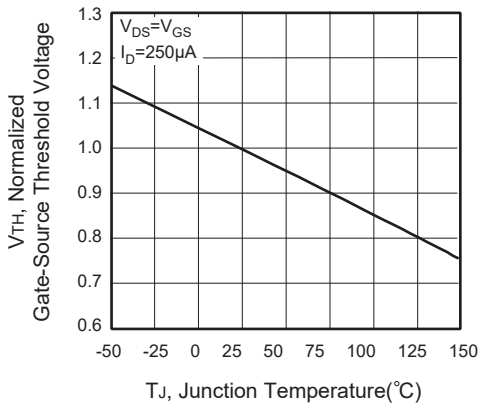


Figure 5. Gate Threshold Variation with Temperature

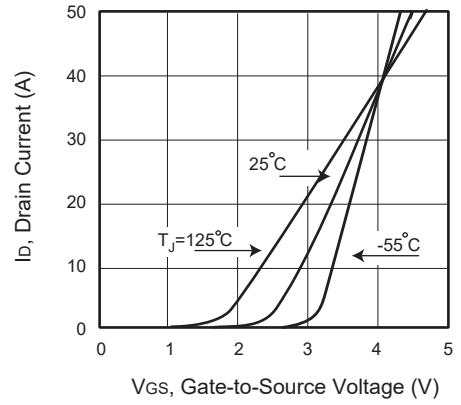


Figure 2. Transfer Characteristics

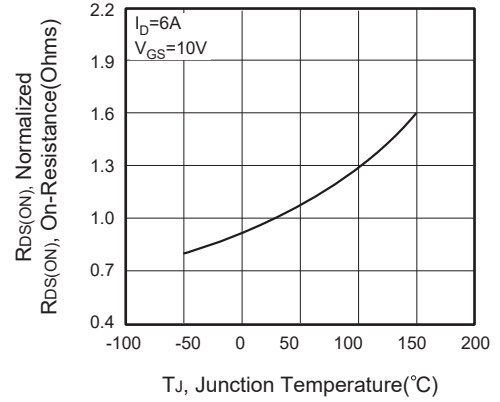


Figure 4. On-Resistance Variation with Temperature

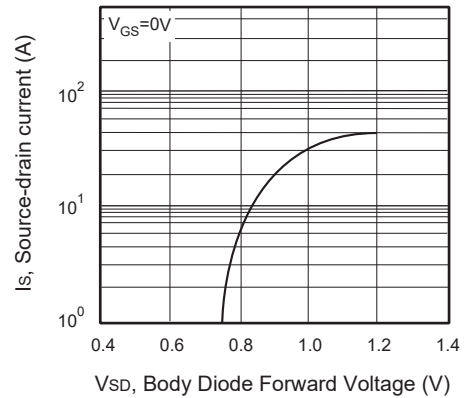


Figure 6. Body Diode Forward Voltage Variation with Source Current

P-CHANNEL

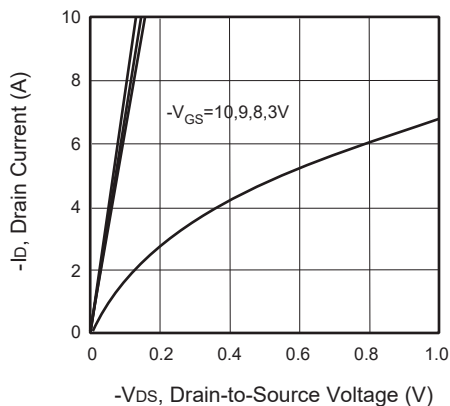


Figure 7. Output Characteristics

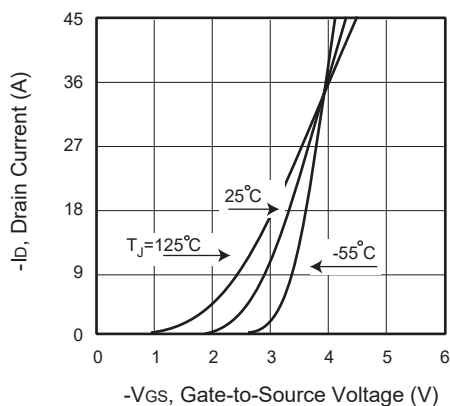


Figure 8. Transfer Characteristics

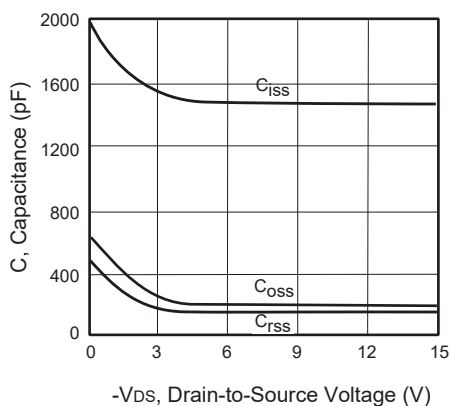


Figure 9. Capacitance

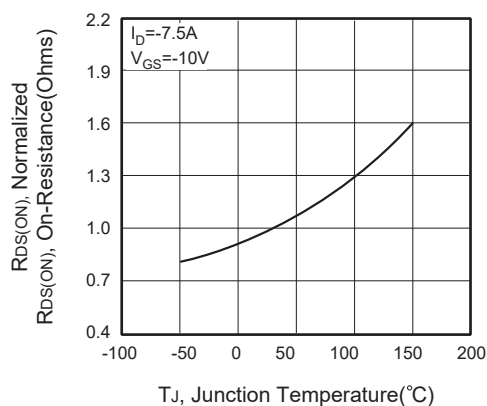


Figure 10. On-Resistance Variation with Temperature

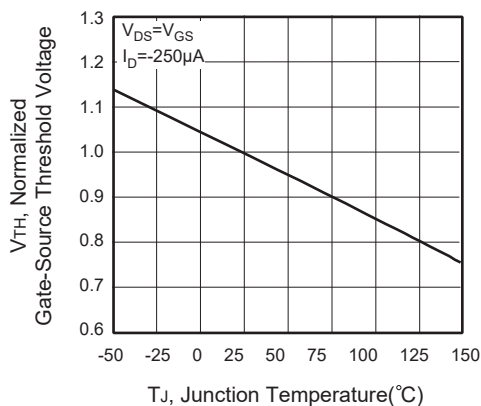


Figure 11. Gate Threshold Variation with Temperature

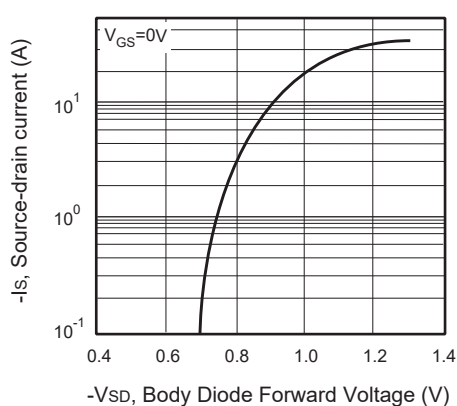


Figure 12. Body Diode Forward Voltage Variation with Source Current

N-CHANNEL

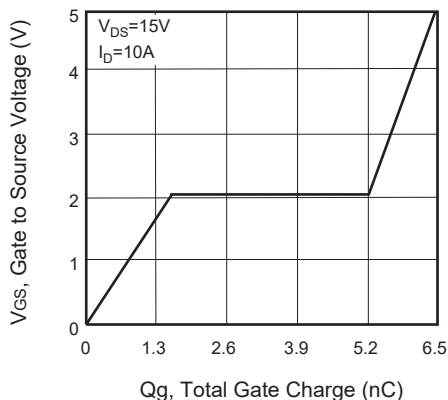


Figure 13. Gate Charge

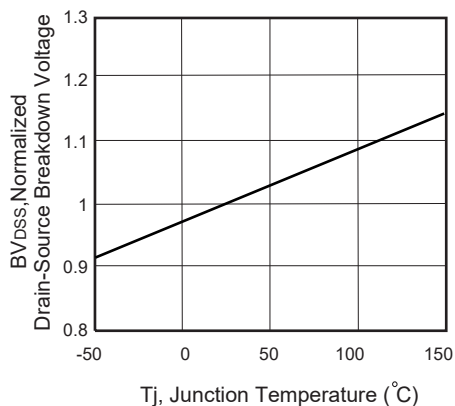


Figure 15. Breakdown Voltage Variation VS Temperature

P-CHANNEL

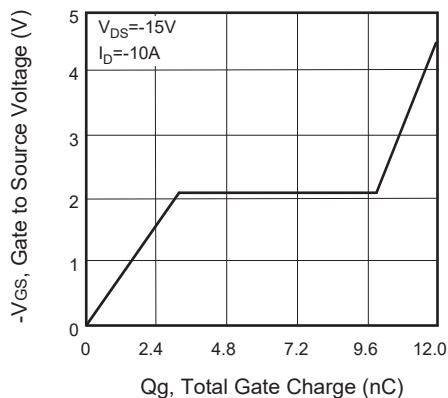


Figure 17. Gate Charge

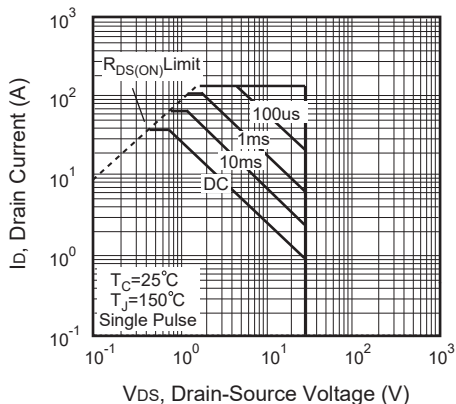


Figure 14. Maximum Safe Operating Area

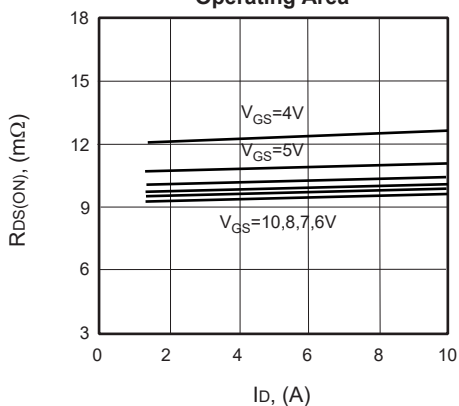


Figure 16. On-Resistance vs. Drain Current

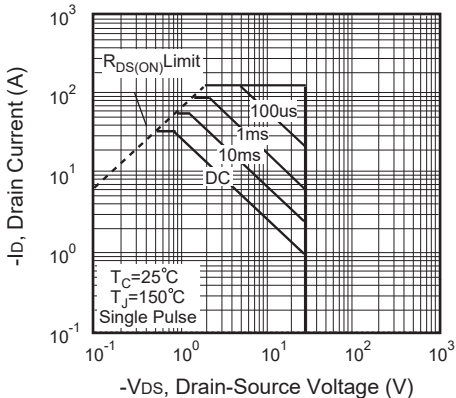


Figure 18. Maximum Safe Operating Area

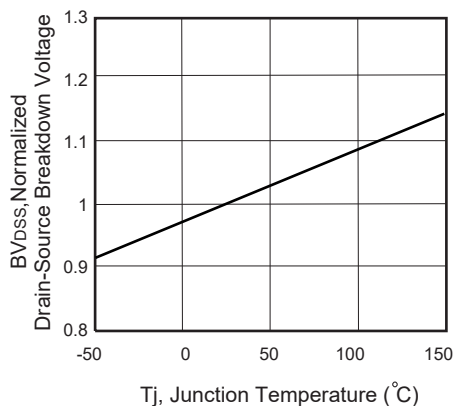


Figure 19. Breakdown Voltage Variation VS Temperature

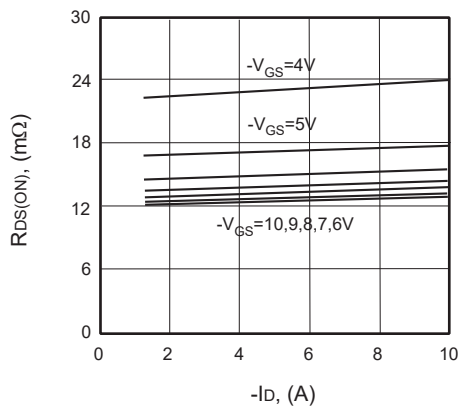


Figure 20. On-Resistance vs. Drain Current

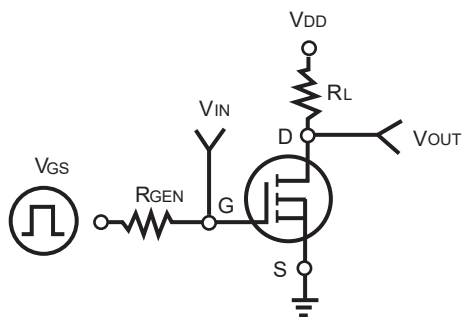


Figure 21. Switching Test Circuit

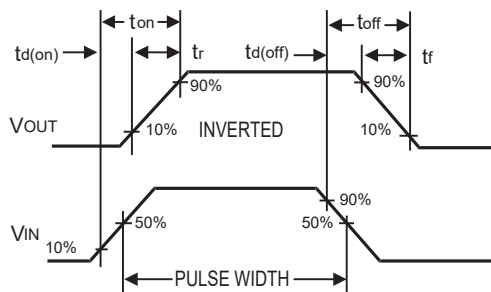


Figure 22. Switching Waveforms

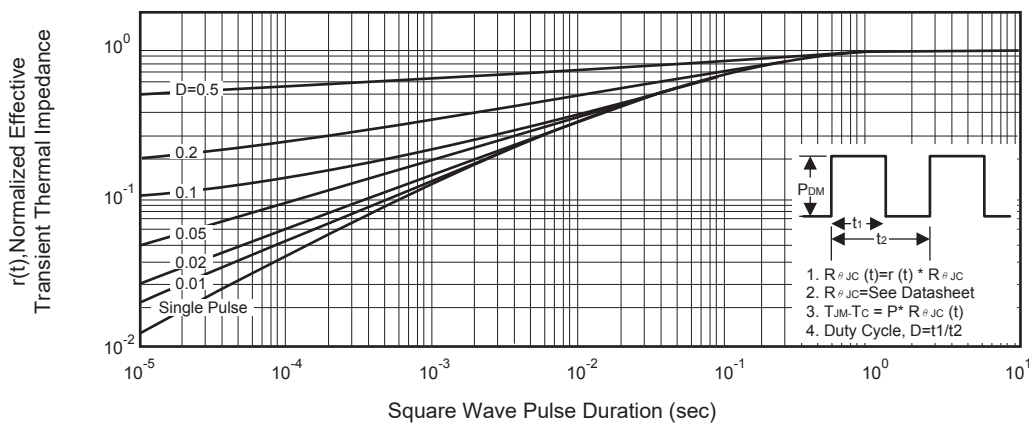
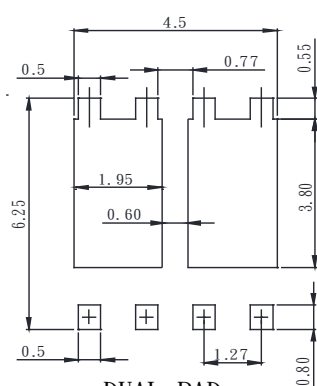
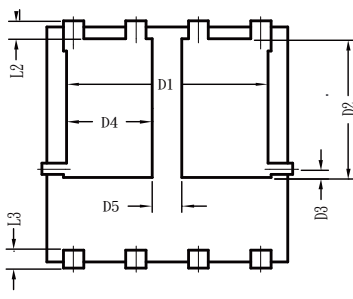
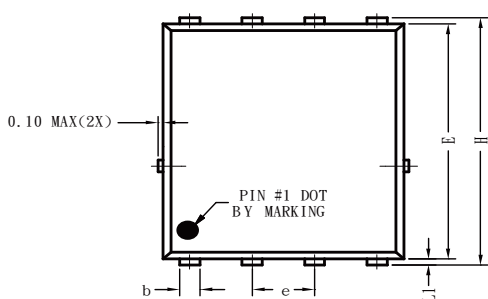


Figure 23. Normalized Thermal Transient Impedance Curve

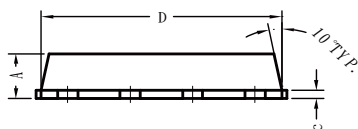
P-PAK5X6 產品外觀尺寸圖 (Product Outline Dimension)

DUAL PAD 尺寸圖



DUAL PAD

RECOMMENDED LAND PATTERN



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.800	1.170	0.031	0.046
b	0.340	0.490	0.013	0.019
c	0.20	0.34	0.008	0.013
D	4.800	5.100	0.009	0.011
D1	3.800	4.200	0.150	0.165
D2	3.180	3.78	0.125	0.149
D3	0.150	0.360	0.006	0.142
D4	1.600	1.800	0.063	0.071
D5	0.500	0.700	0.020	0.028
E	5.650	5.900	0.222	0.232
e	1.270 TYP		0.050 TYP	
H	5.900	6.150	0.232	0.242
L1	0.050	0.250	0.002	0.010
L2	0.380	0.620	0.015	0.024
L3	0.380	0.75	0.015	0.030